Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Original) A probe card for use in probing test of semiconductor integrated circuits arranged on a semiconductor wafer in rows and columns, comprising:

a card substrate;

groups of probe needles, said groups arranged on said card substrate in two columns and at least two rows, to contact connection terminals of semiconductor integrated circuits which are arranged in two columns and at least two rows, and

groups of signal lines, each group of signal lines provided for one group of probe needles, each signal line provided for supplying a test signal from a tester to one probe needle and a response signal from the probe needle to the tester,

wherein a test signal supplied from said tester is supplied from said probe needles to the semiconductor integrated circuits arranged in two columns and at least two rows at the same time through said groups of probe needles, and response signals generated by the semiconductor integrated circuits arranged in two columns and at least two rows are simultaneously supplied to the tester through said groups of probe needles.

2. (Original) The probe card according to claim 1, wherein said card substrate has a rectangular through hole having first and second long sides, the probe needles of the groups extend through the rectangular through hole, the probe needles of some groups are arranged along the first long side of the rectangular hole

to contact the connection terminals of the semiconductor integrated circuits arranged in the first column, and the probe needles of the other groups are arranged along the second long side of the rectangular through hole to contact the connection terminals of the semiconductor integrated circuits arranged in the first column.

3. (Original) The probe card according to claim 1, wherein connection terminals of the semiconductor integrated circuits comprise a plurality of pads which are arranged in at least two columns.

4. (Original) The probe card according to claim 2, which further comprises groups of contacts exposed on a surface of said card substrate, to be connected to the tester, and groups of wires connecting the groups of probe contacts to the groups of probe needles; and in which said probe substrate consists of first and second halves divided along a longitudinal axis of said rectangular hole, the wires connected to the probe needles to contact the connection terminals of the semiconductor integrated circuits arranged in the first column and the probe contacts connected to these wires are provided on the first half of said probe substrate, and the wires connected to the probe needles to contact the connection terminals of the semiconductor integrated circuits arranged in the second column and the probe contacts connected to these wires are provided on the second half of said probe substrate.

5. (Original) The probe card according to claim 4, wherein said probe substrate comprises a plurality of layers, said wires are divided into groups in accordance with types of signals and types of powers, and the groups of wires, thus formed, are provided on the layers, respectively.

6. (Currently Amended) A method for testing semiconductor integrated circuits, the method comprising:

providing a semiconductor wafer having a plurality of semiconductor integrated circuit chips arranged thereon in two columns and at least two rows, each of said plurality of semiconductor integrated chips having a plurality of external terminals;

coupling a probe card to the semiconductor wafer through a plurality of probe needles on said probe card corresponding to said plurality of external terminals of each of said integrated circuit chips, said probe card receiving a plurality of independent test signals and a power supply signal from a tester, wherein said probe card includes structure defining a rectangular through hole having first and second long sides, and wherein the probe needles extend through the rectangular through hole;

concurrently supplying the independent test signals and the power supply signal from the tester through the probe needles to said plurality of external terminals of said plurality of integrated circuits; and

concurrently measuring electric characteristics of said semiconductor integrated circuit chips in an independent manner.

7. (Currently Amended) The method of claim 6, wherein said external terminals are centrally disposed within said integrated circuit chips, with integrated circuits on either side of said external terminals.

8. (Currently Amended) The method of claim 7, wherein said external terminals are arranged in a plurality of columns and rows.

9. (Currently Amended) The method of claim 8, wherein the step of providing a semiconductor wafer includes forming memory arrays for each of said integrated circuit chips.

10. (Currently Amended) The method of claim 6, wherein the test signal and the power supply signal are supplied from said tester to said probe needles by way of a plurality of wiring lines on internal layers of said probe card.

11. (Currently Amended) The method of claim 6, wherein the test signal and the power supply signal are supplied from said tester to said probe needles by way of a plurality of wiring lines on different internal layers of said probe card, said wiring lines positioned on different ones of said different internal layers according to a type of signal carried by said wiring lines.

12. (Currently Amended) A probing test method of semiconductor integrated circuits, comprising:

preparing at least one semiconductor wafer, said semiconductor wafer having a plurality of semiconductor integrated circuit chips arranged thereon in rows and columns, said semiconductor integrated circuit chips having a plurality of external pads;

preparing at least one probe card, said probe card having a plurality of connection terminals for receiving from a tester a test signal and a power supply signal, said at least one probe card having a plurality of probe needles corresponding to said plurality of external pads, respectively, wherein said probe card includes structure defining a rectangular through hole having first and second long sides, and wherein the probe needles extend through the rectangular through hole;

supplying said test signal and said power supply signal from said tester to said probe needles by way of said connection terminals in a completely independent manner;

supplying said test signal and said power supply signal from said probe needles to said semiconductor integrated circuit chips, by way of said external pads, in a completely independent and concurrent manner; and

measuring electric characteristics of the semiconductor integrated circuit chips in a completely independent and concurrent manner.

13. (Previously Presented) The probing test method according to claim 12, wherein said test signal and said power supply signal are supplied from said connection terminals to said probe needles in a completely independent and concurrent manner, by way of a plurality of completely independent wiring lines which are provided inside said probe card and to which said test signal and said power supply terminal are transmitted.

14. (Previously Presented) The probing test method according to claim 12, wherein said test signal and said power supply terminal are supplied from said connection terminals to said probe needles in a completely independent and concurrent manner, by way of a plurality of wiring lines which are provided inside said probe card in accordance with kinds of signals and types of power supplies.

15. (Previously Presented) The probing test method according to claim 12, further comprising:

preparing at least one test station; and

attaching said probe card to said at least one test station.

16. (Previously Presented) The probing method according to claim 12, further comprising:

preparing at least one test station; and

attaching a plurality of probe cards to said at least one test station.